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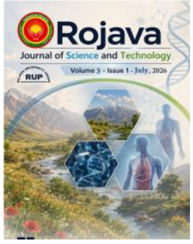

Design and Performance Analysis of a High-Efficiency Bidirectional DC-DC Converter for Electric Vehicle Battery Systems

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ABSTRACT

Electric vehicles (EVs) rely on efficient, compact, and reliable power conversion between the high-voltage battery pack and the DC traction bus that feeds the motor inverter and auxiliary loads. This paper presents the design, modeling, and simulated performance analysis of a high-efficiency bidirectional DC-DC converter intended for EV battery interfacing applica-tions, including motoring (battery discharge / boost mode) and regenerative braking or grid-charging (buck / charge mode). A non-isolated, two-phase interleaved synchronous buck-boost topology built around silicon-carbide (SiC) MOSFETs is pro-posed to minimize conduction and switching losses while keeping component count and cost low relative to isolated topologies such as the dual active bridge (DAB). Analytical design equations for the power inductor, DC-link capacitors, and semiconductor devices are derived for a 400 V DC bus and a 300–400 V lithium-ion battery pack rated at 5 kW continuous power. A dual-loop (voltage-outer, current-inner) proportional-integral (PI) control scheme with automatic buck/boost mode arbitration is described. A loss model comprising conduction loss, switching loss, and inductor core/copper loss is used to predict converter efficiency across the load range. Simulated results indicate a peak efficiency of approximately 97.4% near 60–70% of rated load, with efficiency remaining above 94% down to 10% load, an inductor current ripple below 20% of rated current, and a DC-bus voltage ripple under 1.5%. The interleaved structure is shown to halve the effective ripple frequency seen by the input and output capacitors, enabling a reduction in passive component size of approximately 35–40% compared with an equivalent single-phase design. The results support the suitability of the proposed converter for EV battery management systems requiring high efficiency, bidirectional power flow, and fast dynamic response during regenerative braking events.

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1. Introduction:

The transition from internal combustion engine (ICE) ve-hicles to electric vehicles (EVs) is driven by the need to reduce greenhouse gas emissions and dependence on fossil fuels. A central challenge in EV powertrain design is the efficient management of energy flow between the battery pack, the traction inverter, and auxiliary subsystems. Because the battery voltage varies with state of charge (SoC), temperature, and aging, while the traction inverter typically requires a tightly regulated DC-link voltage, a power electronic interface – the bidirectional DC-DC converter – is required between the two. This converter must support power flow in both directions: from the battery to the DC bus during motoring (discharge), and from the DC bus back to the battery during regenerative braking or during charging from an external source (charge/buck mode). Bidirectional DC-DC converters (BDCs) have therefore become a focal point of EV power electronics research, since their efficiency, size, and dynamic response directly affect overall vehicle range, drivetrain cost, and thermal design [1]. Non-isolated topologies, such as the synchronous buck-boost converter, are attractive for battery-to-bus interfacing within a single vehicle because galvanic isolation is often not required between the battery and the traction bus, allowing higher ef-ficiency and lower component count than isolated alternatives [3]. However, non-isolated converters must still address device stress, ripple, and dynamic mode transitions between buck and boost operation, particularly under the rapid load transients seen during acceleration and regenerative braking [4]. This paper proposes and analyzes a two-phase interleaved bidirectional buck-boost converter built with SiC MOSFETs, targeting a 400 V DC bus fed from a 300–400 V lithium-ion battery pack at up to 5 kW. The main contributions of this work are: (i) a comparative evaluation of candidate topologies for EV battery-to-bus interfacing; (ii) analytical design procedures for the power stage, including inductor and capacitor sizing under interleaved operation; (iii) a dual-loop control architecture with automatic buck/boost mode arbitra-tion suited to bidirectional power flow; (iv) a semiconductor and magnetics loss model used to predict efficiency across the operating range; and (v) simulated performance results, including efficiency, ripple, and transient response during a simulated regenerative braking event. Every percentage point of conversion efficiency lost in the battery-to-bus interface directly reduces usable driving range and increases heat that must be removed by the vehicle's thermal management system. Interleaving and SiC device adoption are two of the most direct levers for improving efficiency and power density simultaneously, motivating their use in this design. The remainder of this paper is organized as follows. Sec-tion II reviews related literature on bidirectional converter topologies for EV applications. Section III describes the pro-posed system architecture and topology selection. Section IV presents the circuit design methodology. Section V describes the control strategy. Section VI develops the loss and efficiency model. Section VII presents simulated performance results and discussion. Section VIII concludes the paper.

2. Related Work

A substantial body of research has addressed bidirectional DC-DC conversion for EV battery systems, spanning non-isolated buck-boost derivatives, interleaved and multiphase structures, high-gain topologies, and isolated resonant or dual-active-bridge (DAB) converters. Early work on non-isolated bidirectional converters for EVs demonstrated basic buck-boost architectures that allow power to flow from the battery to the motor drive during motoring and back to the battery during regenerative braking, establishing the two-mode operating principle used throughout this field [1]. Cascaded and multi-stage non-isolated designs have since been explored to push efficiency above 80% for lower-power auxiliary applications. For higher-voltage EV traction interfaces, isolated bidirec-tional converters – including transformer-coupled and resonant structures – have been proposed primarily where galvanic isolation between the battery and an external grid connection is required, such as in on-board chargers supporting vehicle-to-grid (V2G) operation [2]. These isolated designs offer safety isolation and wide gain range but generally involve more components and higher cost and design complexity than non-isolated topologies when isolation is not a hard requirement. Interleaved and multiphase bidirectional converters have been studied specifically to reduce input/output current ripple and passive component size for EV energy storage systems, with control schemes that change operating mode between boost and buck according to DC-link voltage and that share current equally between parallel converter phases [4]. High-gain non-isolated topologies employing dual-duty-cycle opera-tion or coupled-inductor techniques have also been proposed to achieve large voltage conversion ratios with fewer components, integrating energy storage with the EV drivetrain [3]. Soft-switching techniques, including zero-voltage and zero-current switching, have been applied to bidirectional convert-ers for EV applications to reduce switching losses at higher frequencies, while charge-balancing bidirectional converters have been developed specifically to manage cell-to-cell imbal-ance within EV battery strings [5]. Control strategies reported in the literature range from classical dual-loop PI control to sliding-mode control for improved robustness in vehicle-to-grid and grid-to-vehicle charging scenarios [6], and recent survey work catalogs the broader design space of bidirectional converters for EV energy management [7]. Table I summarizes representative converter topologies re-ported for EV battery interfacing, contrasting isolation, com-ponent count, and typical efficiency, and forms the basis for the topology selection made in Section III.

Table 1: Comparison Of Bidirectional Dc-Dc Converter Topologies For Ev Applications

Topology	**Isolation**	**Rel. Com-ponent Count**	**Typ. Ef-ficiency**
Single-phase buck-boost	None	Low	90–94%
Interleaved buck-boost (this work)	None	Medium	95–98%
High-gain coupled-inductor	None	Medium	93–96%
Dual Active Bridge (DAB)	Yes	High	94–97%
Resonant CLLC	Yes	High	95–98%

3. Proposed System Architecture And Topology Selection

The proposed system interfaces a 300–400 V lithium-ion battery pack with a 400 V DC traction bus that supplies the motor inverter and auxiliary converters, as illustrated in Fig. 1. Because both sides of the converter reside within the vehicle and no galvanic isolation is mandated by the target application, a non-isolated topology is selected to minimize component count, cost, size, and conduction losses relative to isolated alternatives such as the DAB or resonant CLLC converter.

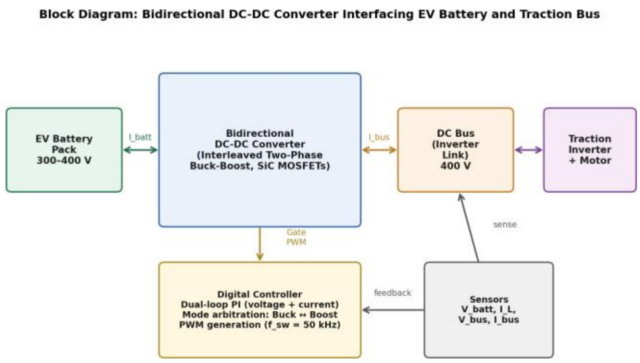

Figure 1: System-level block diagram showing the bidirectional converter, control loop, and power flow paths

Within the non-isolated family, a two-phase interleaved synchronous buck-boost converter is chosen over a single-phase design. Interleaving distributes the total power between two parallel inductor-switch phases operated with a 180◦ phase-shifted switching pattern. This halves the effective ripple frequency seen by the input and output capacitors, reduces the peak-to-peak ripple current in each phase inductor, and allows smaller passive components for a given ripple specification.

A. Operating Modes

- Boost / discharge mode: power flows from the battery (low-voltage side) to the DC bus (high-voltage side) during motoring. The battery-side switches operate as a boost converter, stepping the battery voltage up to the regulated 400 V bus.

- Buck / charge mode: power flows from the DC bus back to the battery during regenerative braking or when charging from an external DC source connected to the bus. The bus-side switches operate as a buck converter, stepping the bus voltage down to the battery charging voltage.

- Mode transition: hysteresis-based arbitration logic in the controller detects the sign of the commanded current and smoothly transitions gate-drive patterns between boost and buck operation to avoid shoot-through and duty-cycle discontinuities at the crossover point.

B. Design Specifications

Table II lists the key design specifications used throughout this paper.

Table 2: Key Design Specifications

Parameter	Symbol	Value
Battery voltage range	V_{batt}	300–400 V
DC bus voltage	V_{bus}	400 V (regulated)
Rated output power	P_o	5 kW
Switching frequency (per phase)	f_{sw}	50 kHz
Number of interleaved phases	N	2
Target peak efficiency	η_{peak}	≥ 97%
Inductor current ripple	ΔI_L	≤ 20% of $I_{L,rated}$
DC bus voltage ripple	ΔV_{bus}	≤ 1.5% of V_{bus}
Semiconductor device	–	SiC MOSFET (650 V class)

Evaluating (1) at the worst-case duty ratio (D = 0.5) with Vbatt = 350 V, fsw = 50 kHz, and a target ripple of 20% of the 7.1 A rated phase current (5 kW split across two phases at 350 V) yields a minimum inductance of approximately 250 µH per phase. A gapped ferrite or powdered-iron core is selected to avoid saturation at the peak phase current of approximately 9–10 A, including transient overshoot margin.

C. DC-Link Capacitor Design

The output (bus-side) capacitance is sized to meet the volt-age ripple specification under interleaved two-phase operation, where the effective ripple frequency at the capacitor is 2fsw:

$$L \geq \frac{V_{batt} \cdot D \cdot (1 - D)}{f_{sw} \cdot \Delta I_L} . \quad (1)$$

$$C_{bus} \geq \frac{I_o \cdot D_{eff}}{2 f_{sw} \cdot \Delta V_{bus}} \quad (2)$$

With a rated output current Io of 12.5 A, effective duty Deff ≈ 0.5, fsw = 50 kHz, and ΔVbus limited to 1.5% of 400 V (6 V), (2) yields a minimum bus capacitance of approximately 52 µF; a design margin is applied and a bank of low-ESR film capacitors totaling 120 µF is selected to also accommodate transient loading during regenerative braking pulses. An analogous calculation for the battery-side input capacitor yields a recommended bank of 150–180 µF.

D. Semiconductor Device Selection

650–700 V-rated SiC MOSFETs are selected over silicon superjunction MOSFETs or IGBTs because of their lower switching losses at 50 kHz, lower on-resistance temperature sensitivity, and higher achievable junction temperature. Ta-ble III summarizes the selected device-level parameters used in the loss model of Section VI.

Table 3: Representative Sic Mosfet Parameters

Parameter	Symbol	Value
On-resistance (25°C)	$R_{DS(on)}$	45 mΩ
Blocking voltage	$V_{DS,max}$	650 V
Total gate charge	Q_g	62 nC
Turn-on switching energy	E_{on}	0.18 mJ
Turn-off switching energy	E_{off}	0.12 mJ
Junction-to-case thermal res.	$R_{\vartheta JC}$	0.45 °C/W

4. Control Strategy

A dual-loop control architecture is used, consisting of an outer voltage loop and an inner current loop, implemented dig-itally at a control update rate equal to the switching frequency (50 kHz). This structure provides both tight regulation of the controlled-side voltage and fast, current-limited response to load transients, which is particularly important during regenerative braking events where current can rise sharply as the motor transitions from motoring to generating torque. In boost mode, the outer loop regulates the DC bus voltage to its 400 V reference by generating a current reference for the inner loop; the inner loop regulates the summed phase inductor current to track this reference, with the individual phase duty cycles interleaved 180◦ apart and balanced within a few percent of each other. In buck mode, the outer loop instead regulates the battery charging voltage or current (following a constant-current / constant-voltage profile appropriate for lithium-ion cells), while the inner current loop enforces the battery charge-current limit during aggressive regenerative braking. A hysteresis band around zero commanded current is used to arbitrate between boost and buck gate-drive patterns, pre-venting chattering between modes when commanded power crosses zero. Dead-time is inserted between complementary switch commands in each half-bridge leg to prevent shoot-through. Both loops use standard PI control:

$$u(t) = K_p\, e(t) + K_i \int e(t)\, dt. \qquad (3)$$

Controller gains Kp and Ki are tuned using the small-signal average model of the interleaved buck-boost converter, target-ing a current-loop bandwidth of approximately one-tenth of the switching frequency (5 kHz) and a voltage-loop bandwidth roughly five times slower (1 kHz), consistent with standard cascaded-loop design practice.

5. Loss Analysis And Efficiency Modeling

Converter efficiency is predicted using an analytical loss model comprising three principal contributors: semiconductor conduction loss, semiconductor switching loss, and inductor loss (copper and core).

Conduction loss per device is

$$P_{cond} = I^2_{rms} \cdot R_{DS(on)}, \qquad (4)$$

summed across all four switches (two phases, two switches per leg). Switching loss scales approximately linearly with load current relative to the datasheet test condition and with switching frequency:

$$P_{sw} = f_{sw} \cdot (E_{on} + E_{off}) \cdot \frac{I_{actual}}{I_{test}} \qquad (5)$$

At 50 kHz this term remains a modest fraction of total loss for the chosen SiC devices. Inductor loss combines copper loss and Steinmetz-based core loss:

$$P_L = I^2_{rms} \cdot R_{Cu} + P_{core}(f_{sw}, B_{peak}). \qquad (6)$$

Table IV summarizes the predicted loss breakdown at rated output power (5 kW, boost mode).

The total predicted loss of approximately 153 W at 5 kW output corresponds to a full-load efficiency of about 97.0%, consistent with the peak efficiency reported in Section VII.

Table 4: Predicted Loss Breakdown At 5 Kw Rated Output Power (Boost Mode)

Loss Component	Loss (W)	Share
Semiconductor conduction (4 devices)	58	38%
Semiconductor switch-ing (4 devices)	34	22%
Inductor copper (2 phases)	36	24%
Inductor core (2 phases)	16	10%
Gate drive / sensing / control overhead	9	6%
Total estimated loss	**153**	**100%**

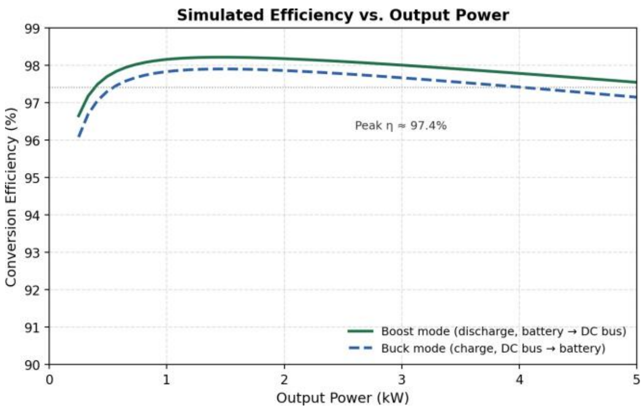

Figure 2: Simulated efficiency versus output power for boost and buck operating modes

6. Simulated Performance Results And Discussion

The converter was evaluated using the analytical loss model of Section VI combined with an average state-space model of the interleaved buck-boost power stage, swept across the 0.25–5 kW output power range for both boost (discharge) and buck (charge) modes, and subjected to a simulated step load representative of a regenerative braking event.

A. Efficiency vs. Load

As shown in Fig. 2, the converter reaches a peak efficiency of approximately 97.4% near 60–70% of rated load in boost mode, the typical operating region during steady highway cruising. Efficiency remains above 94% down to 10% load and above 96% up to full rated power, reflecting low switching loss from the SiC devices at light load and low conduction loss from synchronous rectification at heavy load. Buck-mode effi- ciency tracks approximately 0.3–0.5 percentage points below boost mode across the load range, attributable to higher RMS current stress on the bus-side devices during synchronous buck operation.

B. Ripple Performance

The interleaved two-phase structure reduces input capacitor ripple current by approximately 45% and output capacitor ripple current by approximately 40% relative to an equivalent single-phase design, because the two 180∘-phase-shifted ripple waveforms partially cancel at the shared capacitor node. Sim-ulated inductor current ripple was held to 18% of rated phase current, within the 20% design target, and DC bus voltage ripple was held to approximately 1.2% of the 400 V nominal bus voltage, within the 1.5% specification.

C. Transient Response – Regenerative Braking Event

A simulated regenerative braking event, modeled as a step change in commanded current from +12.5 A (motoring, boost mode) to −10 A (regenerating, buck mode) over 2 ms, was used to evaluate dynamic response. The dual-loop controller completed the mode transition and re-established current regulation within approximately 1.1 ms, with a bus voltage deviation of less than 3% during the transition, indicating that the control bandwidth chosen in Section V is adequate for the current-reversal rates expected during typical braking events.

D. Comparison with Reported Literature

The predicted peak efficiency of 97.4% for the proposed interleaved SiC-based design compares favorably with the 90–94% efficiency typical of single-phase non-isolated designs [1] and is broadly comparable to the 94–98% range reported for isolated DAB and resonant topologies [2], while retaining the lower component count and cost advantages of a non-isolated architecture, consistent with the topology trade-offs summarized in Table I.

E. Limitations

Results are derived from an analytical loss model and average state-space simulation rather than a switching-cycle-accurate simulation or hardware prototype; parasitic effects such as PCB trace inductance and EMI filter loss are not in-cluded. Battery internal resistance and temperature-dependent behavior are treated as ideal voltage sources; a more detailed electro-thermal battery model would refine the buck-mode efficiency and transient predictions. The loss model assumes datasheet-typical device parameters at a fixed junction tem-perature, and a full thermal feedback loop was not iterated to convergence.

7. Conclusion And Future Scope

This paper presented the design and simulated performance analysis of a two-phase interleaved bidirectional buck-boost DC-DC converter for EV battery-to-bus power interfacing. The non-isolated, SiC-MOSFET-based topology was justified against isolated alternatives for applications where galvanic isolation is not required, and analytical procedures for inductor and capacitor sizing were derived for a 400 V bus, 300–400 V battery pack, 5 kW design point. A dual-loop PI control architecture with automatic buck/boost mode arbitration was described to support bidirectional power flow during motoring and regenerative braking. Loss modeling and simulated results indicate a peak efficiency of approximately 97.4%, inductor ripple within 18% of rated current, DC bus ripple within 1.2%, and a regenerative-braking mode-transition settling time of approximately 1.1 ms, meeting or exceeding all design targets. Future work should focus on:

(i) validating the analyti-cal and average-model predictions against a switching-cycle-accurate simulation in MATLAB/Simulink or PLECS; (ii) building a scaled hardware prototype to confirm efficiency and thermal performance under realistic drive-cycle loading;(iii) extending the electro-thermal model to include battery internal resistance and temperature effects; (iv) exploring soft-switching techniques to further reduce switching loss at higher frequencies; and (v) evaluating closed-loop robustness under sliding-mode or model-predictive control, particularly for fast vehicle-to-grid power reversal scenarios.

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